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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,037	09/24/2003	Edmund Burke	TI-33719	5055

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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,037	BURKE ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 16-34* is/are rejected.

7)☒ Claim(s) *9-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-24-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to filling of the application on September 24, 2003. Claims 1-34 are pending.

*** In claim 9, line 6, the term "grater" should be --greater--.

*** Specification page 1, updating information of related application is respectfully requested.

Claim Rejections - 35 USC § 112

1. Claims 17,33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 17, "...wherein the first region of the first metal layer..." is lacking proper antecedent basis (note claim 17 is similar to claims 10, but dependent differently).

Re claim 33, meaning and scope of the claim are unclear and indefinite as claim 33 recites "second capacitor comprising polysilicon" while base claim 32 differently recites "second capacitor plate comprising a semiconductor well".

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-8,16,17,23,27-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (5,851,868) .

Kim teaches a capacitive structure comprising: a semiconductor base region (21 in Fig2; 51 in Fig 9) having an upper surface; a well 23,54 forming within the semiconductor base

region 21 and adjacent the upper surface (col 3, lines 51-65; Figs 2,9; and well as a second capacitor plate in claims 23,32); the first dielectric layer (25 in Fig 2; 55 in Fig 9) adjacent at least a portion of the upper surface; a polysilicon layer (27 in Fig 2; 59 in Fig 9; col 3, lines 55 through col 4; col 5, lines 1-65; as a first capacitor plate in claims 23,32) adjacent the first dielectric layer, wherein the well, the first dielectric layer, and the first polysilicon layer form a first capacitor and are aligned along a planar dimension (Figs 2-4,9); a first conductive layer (35 in Fig 2; 73 in Fig 9, Fig 6; col 5, lines 46-59; as third capacitor plate in claims 23,32) positioned with at least a portion overlying at least a portion of the polysilicon layer 27,59; a second dielectric layer 37,77 adjacent the first conductive layer; and a second conductive layer 39,79 (as a second capacitor plate in claims 23,32) adjacent the second dielectric layer, wherein the first conductive layer, the second dielectric layer, and the second conductive layer form a second capacitor and are aligned along the planar dimension (Figs 2,9; col 4, lines 45-65; col 6, lines 60 through col 7). Re further claims 2,23, and 32, as shown in Figs 2 and 9, wherein an electrical connection located in contact hole (33 in Fig 2; col 4, lines 15-35 ; 71 in Figs 5,6,9; col 5, lines 45-59) between the polysilicon layer 27,59 (first capacitor plate in claims 23,32) and the first conductive layer 35, 73 (third capacitor plate in claims 23,32). Re claim 3, as shown in Figs 2,9, wherein the first conductive layer 35,73 has a first side adjacent the second dielectric layer 37,77 and a second side facing in a direction toward the upper surface; and wherein the electrical connection contacts the second side of the first conductive layer 35,73 through the contact hole (33 in Fig 2; col 4, liens 15-35 ; 71 in Figs 5,6,9; col 5, lines 45-59). Re claim 4, wherein the electrical connection through the contact hole (33 in Fig 2; col 4, lines 15-35 ; 71 in Figs 5,6,9; col 5, lines 45-59) is substantially perpendicular to the planar dimension. Re claims 5 and 29, wherein the electrical connection comprises a first electrical connection through the contact hole (33 in Fig 2; col 4, lines 15-35 ; 71 in Figs 5,6,9; col 5, lines 45-59), and further comprises a second electrical connection (45 in Fig 2, col 4, lines 35-50; 89 in Fig 9; col 6, lines 4-16) between the second conductive layer and the well. Re claims 6 and 30, wherein the well 23,54 comprises a length having a first end 29,63 and a second end 29,63; wherein the second electrical connection 45,89 is between the second conductive layer and the first end of the well; and wherein the second end of the well is for connecting to fixed potential (Figs 2,9; col 4, lines 25-65). Re claim 7, wherein the fixed potential is ground (GND at col 4, lines 25-65; Figs 2,9).

Re claims 8 and 31, wherein the fixed potential equals to first fixed potential and the first electrical connection is for connecting to a second fixed potential of VCC that is unequal to the first fixed potential of GND (Figs 2,9; col 4, lines 25-65 for VCC). Re claim 16, wherein the semiconductor base region is selected form a set consisting of a semiconductor well 23 and a semiconductor substrate 21 (Fig 2; col 4, lien 45 through col 4). Re claim 17, wherein the second conductive layer 39,79 has a first length in a first dimension along a planar dimension and a first width in a second dimension along the planar dimension that is perpendicular to the first length; wherein the first region of the first metal layer 47 has a second length, less than the first length and in the first dimension; and wherein the first region of the first metal layer has a second width less than the first width and in a second dimension. Re further claim 27, wherein the first capacitor is fixed position relative to the semiconductor substrate; and wherein the second capacitor is in fixed position that at least partially overlies the first capacitor (see Fig 2,9; at least col 3, line 51 through col 4). Re further claim 28, wherein the electrical connection contacts a surface of the third capacitor plate (as a first conductive layer 35 in Fig 2; 73 in Fig 9, Fig 6; col 5, lines 46-59) that faces the semiconductor substrate. Re claim 33, insofar as understood, forming the capacitor plate 59 comprising polysilicon comprised forming a gate region 61 for a transistor proximate the capacitive structure (Figs 2,3,4,9; col 5, lines 1-45, col 4). Re claim 34, wherein forming a dielectric 55 between the first capacitor plate 59 and the second capacitor plate 54 comprises forming a gate insulator 57 for a transistor proximate the capacitive structure (Figs 3-4,2,9; col 5, lines 1-45; col 4).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (5,851,868) taken with Wu (5,998,264).

Kim teaches a capacitive structure as applied to claims 1-8,16,17,23,27-34 above.

Re claims 11-15, Kim lacks using TaN for forming the first and second conductive layers (as third and fourth capacitor plate in claim 24); and using Ta_2O_5 for the second dielectric, with dielectric constant greater than 4.0 to form the second capacitor having greater capacitance.

However, Wu teaches (at Figs 8-10; col 6, lines 15-51) forming the second capacitor by using a conductive material including TaN for forming the first and second conductive layers (as third and fourth capacitor plate in claim 24); and by using Ta_2O_5 material for forming the second dielectric (col 6, lines 28-40), wherein the Ta_2O_5 has a dielectric constant greater than 4.0, inherently, wherein the second capacitor formed as a MIM with high-k dielectric layer has a capacitance greater than that of the underlying first capacitor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the second capacitor of Kim by using TaN for first and second conductive layers (as third and fourth capacitor plate in claim 24) and by using Ta_2O_5 for the second dielectric, with dielectric constant greater than 4.0, as taught by Wu. This is because of the desirability to form a thinner capacitor but having greater capacitance so that high density flash memories with MIM structure can be manufactured.

Allowable Subject Matter

*** Claims 9-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*** The following is a statement of reasons for the indication of allowable subject matter:

The references including Kim (5,851,868), Wu (5,998,264), of record, alone or in combination, do not fairly anticipatively disclose each and every aspect of the claimed capacitive

structure, or fairly make a prima facie obvious case of the claimed capacitive structure, in combination with other claimed limitations, and further inclusion of limitations in claim 9.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 8:30 Am to 5:00 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-16

Michael Trinh
Primary Examiner